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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,198	06/27/2001	Ramkumar Subramanian	F0656	3867

23623 7590 07/21/2004

AMIN & TUROCY, LLP
1900 EAST 9TH STREET, NATIONAL CITY CENTER
24TH FLOOR,
CLEVELAND, OH 44114

EXAMINER	
BERRY, RENEE R	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,198	SUBRAMANIAN ET AL.	
	Examiner	Art Unit	
	Renee R Berry	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) 15-17 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 and 18-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 June 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 and 18-25 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,753,250 to Hill et al.

In regards to claim 1, Hill teaches a method of forming copper features on a semiconductor substrate, comprising: coating the substrate with a copper seed layer to form a composite; coating the composite with a resist;
exposing the resist to actinic radiation; developing the resist to expose a portion of the copper seed layer and form a patterned resist coating; and
plating copper to obtain copper features grown from the copper seed
layer at column 8, lines 15-28.

In regards to claim 2, Hill teaches stripping the resist after plating the copper; forming a dielectric coating over the copper features; and removing a portion of the dielectric coating to expose the copper features at column 8, lines 5-14.

In regards to claim 3, Hill teaches the portion of the dielectric coating is

removed by mechanical polishing at column 8, lines 36-38.

In regards to claim 4, Hill teaches the portion of the dielectric coating is removed by chemical-mechanical polishing at column 8, lines 43-49.

In regards to claim 5, Hill teaches prior to coating with the dielectric, coating the copper features with a diffusion barrier forming material at column 7, lines 51-57 and column 8, lines 15-20.

In regards to claim 6, Hill teaches prior to stripping the resist, planarizing the copper features and the patterned resist coating at column 8, lines 4-10.

In regards to claim 7, Hill teaches after developing but prior to plating, trimming the patterned resist coating to increase a line width defined by an opening in the patterned resist coating at column 7, lines 424-30.

In regards to claim 8, teaches trimming increases the line width by at least about 25%.

In regards to claim 9, Hill teaches a method of forming copper features on a semiconductor substrate, comprising: coating the semiconductor substrate with a resist; exposing the resist to actinic radiation; developing the resist to form a patterned resist coating having openings, forming a copper seed layer over the patterned resist coating and substrate to form a composite; removing a portion of the copper seed layer outside of the openings; plating copper to obtain copper features grown from the copper seed layer within the openings of the patterned resist coating at column 7, lines 20-25 and column 8, lines 15-29.

In regards to claim 10, Hill teaches stripping the resist; coating the copper and the exposed substrate with a dielectric; and removing a portion of the dielectric to expose the copper at column 8, lines 5-15.

In regards to claim 11, Hill teaches prior to coating with the dielectric, coating the copper with a diffusion barrier forming material at column 8, lines 15-19.

In regards to claim 12, Hill teaches prior to stripping the resist, planarizing the copper features and the resist at column 8, lines 5-12.

In regards to claim 13, Hill teaches after developing but prior to plating, trimming the patterned resist coating to increase a line width defined by an opening in the patterned resist coating at column 8, lines 5-12.

In regards to claim 18, Hill teaches a method of forming copper features on a semiconductor substrate, comprising: coating the substrate with a copper seed layer to form a composite; coating the composite with a resist; exposing the resist to actinic radiation; developing the resist to form a patterned resist coating having openings; and coating the resist with a dielectric that fills the openings; polishing to remove dielectric outside the openings; stripping the resist to expose a portion of the copper seed layer; and plating copper to obtain copper features grown from the copper seed layer at column 8, lines 15-29.

In regards to claim 19, Hill teaches planarizing the copper features and the dielectric at column 8, lines 36-42.

In regards to claim 20, Hill teaches trimming the dielectric prior to plating to increase a line width defined by an opening in the patterned resist coating at colun 8, lines 5-12 and column 7, lines 15-30.

In regards to claim 22, Hill teaches forming copper features on a semiconductor substrate, comprising: coating the substrate with a copper seed layer to form a composite; coating the composite with a resist; exposing the resist to actinic radiation; developing the resist to form a patterned resist coating having openings; and coating the patterned resist with a temporary coating that tills the openings in the patterned resist; polishing to remove the temporary coating outside the openings in the patterned resist; stripping the resist to expose a portion of the copper seed layer; and plating copper to obtain copper features grown from the copper seed layer; stripping the temporary coating; coating the copper features with a dielectric; and polishing to expose the copper features at column 8, lines 5-12.

In regards to claim 23, Hill teaches trimming the temporary coating prior to plating to increase a line width defined by an opening in the temporary coating at column 8, lines 5-10.

In regards to claim 25, Hill teaches prior to coating with the dielectric; coating the copper features with a diffusion barrier forming material at column 8, lines 15-21.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R Berry whose telephone number is (571) 272-1774. The examiner can normally be reached on M-F 9-5:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RRB

David Nelms
Supervisory Patent Examiner
Technology Center 2800

March 24, 2004